dation of silicon (LOCOS) process. In order to fabricate the semiconductor device shown in FIG. **2**, the length of the first isolation region **130** may be made equal to or greater than the length of the second isolation region **230**.

[0129] Referring to FIG. **27**, the P-type base region **295** may be formed between the P-type insulation layer **300** and the N-type second drift region **220** in the second region II. For example, a mask pattern (not shown) having a region defined therein may be formed on the N-type epitaxial layer **200**, and the region may be a potential region for forming the P-type base region **295**. Then, P-type impurity may be implanted into the substrate **10**, the mask pattern may be removed, and the P-type base region **295** may be formed. In an exemplar embodiment in which the semiconductor device is formed on the substrate **10** having a CMOS device thereon, the P-type base region **295** may be formed at the same time when a P-type well of the CMOS device is formed. A doping concentration of the N-type impurity for forming the P-type base region **295** may be in a range of about 1×10^{16} to about 5×10^{17} atoms/cm^3. The range for the N-type impurity concentration may be within a narrower range that includes, but is not limited to, e.g., about 2×10^{16} to about 4×10^{17} atoms/cm^3, about 5×10^{16} to about 1×10^{17} atoms/cm^3, about 9×10^{16} to about 3×10^{17} atoms/cm^3, etc.

[0130] Referring to FIG. **28**, the first gate insulation layer **133** and the first gate **180** may be formed on the N-type first drift region **120** and the first isolation region **130**. The second gate insulation layer **233** and the second gate **280** may be formed on the N-type second drift region **220** and the second isolation region **230**. For example, a pre-gate insulation layer made of, e.g., silicon oxide, and a pre-gate made of, e.g., polysilicon, may be sequentially stacked on the substrate **10**. Next, the pre-gate insulation layer and the pre-gate may be patterned to form the first gate insulation layer **133** and the first gate **180**, and the second gate insulation layer **233** and the second gate **280**, respectively.

[0131] Referring to FIG. **29**, the P-type first body region **151** may be formed at one side of the first gate **180**, and the P-type second body region **251** may be formed at one side of the second gate **280**. For example, mask patterns (not shown) having regions defined therein may be formed, and the regions may be potential regions for forming the P-type first body region **151** and the P-type second body region **251**. Then, P-type impurity may be implanted into the substrate **10**, the mask patterns may be removed, and the P-type first body region **151** and the P-type second body region **251** may be formed. A doping concentration of the P-type impurity for forming the P-type first body region **151** and the P-type second body region **251** may be in a range of about 5×10^{16} to 8×10^{17} atoms/cm^3. The range for the N-type impurity concentration may be within a narrower range that includes, but is not limited to, e.g., about 6×10^{16} to about 7×10^{17} atoms/cm^3, about 9×10^{16} to about 4×10^{17} atoms/cm^3, about 1×10^{17} to about 3×10^{17} atoms/cm^3, etc.

[0132] Referring again to FIG. **2**, P-type impurity may be implanted into the substrate **10** to form the P-type first body contact region **125** in the P-type first body region **151** and to form the P-type second body contact region **252** in the P-type second body region **251**. Then, N-type impurity may be implanted to form the N-type first source region **160**, the N-type first drain region **170**, the N-type emitter region **290**, and the N-type second drain region **270**.

[0133] Methods of fabricating a semiconductor device according to other exemplary embodiments may be inferred by one skilled in the art from the exemplary method depicted in FIGS. **22** to **29**. For example, the following description will focus on differences between the fabrication methods of other exemplary embodiments.

[0134] In the fabricating method of the semiconductor device shown in FIG. **4**, the overlapping length O**2** between the second isolation region **230** and the P-type second deep well **240** may be equal to or greater than the overlapping length O**1** between the first isolation region **130** and the P-type first deep well **140**.

[0135] In the fabricating method of the semiconductor device shown in FIG. **5**, a predetermined portion of the P-type second deep well **240** may overlap with the P-type base region **295**.

[0136] In the fabricating method of the semiconductor device shown in FIG. **6**, the stage of forming the P-type base region **295** shown in FIG. **27** may be omitted, and the P-type second body region **251** may be formed to surround the N-type emitter region **290**.

[0137] In the fabricating method of the semiconductor device shown in FIG. **7**, N-type impurity may be implanted into the substrate **10** to from the N-type second source region **260**, e.g., during a stage of forming the N-type first source region **160**, the N-type first drain region **170**, the N-type emitter region **290**, and the N-type second drain region **270**.

[0138] In the fabricating method of the semiconductor device shown in FIG. **9**, P-type impurity may be implanted into the substrate **10** to form the P-type emitter region **493**, e.g., during a stage of forming the P-type first body contact region **152** and the P-type third body contact region **452**. Further, N-type impurity may be implanted into the substrate **10** to form the N-type impurity region **491**, e.g., during a stage of forming the N-type first source region **160**, the N-type first drain region **170**, the N-type emitter region **490**, and the N-type third drain region **470**.

[0139] Methods of fabricating a semiconductor device according to other exemplary embodiments may be inferred by one skilled in the art from the exemplary method depicted in FIGS. **22** to **29** and in view of the about description with respect to FIGS. **4** to **7**. For example, a method of fabricating the semiconductor device according to the exemplary embodiments shown in FIGS. **11** to **14** may be inferred.

[0140] In an exemplary method of fabricating the semiconductor device shown in FIG. **16**, the fourth isolation region **435** may be formed when the first isolation region **130** and the third isolation region **430** are formed. Further, P-type impurity may be implanted into the substrate **10** to form the P-type emitter region **493** and the P-type base contact region **497**, during, a stage of forming the P-type first body contact region **152** and the P-type third body contact region **452**.

[0141] A fabricating method of the semiconductor device according to the embodiment shown may be inferred from, e.g., the exemplary method depicted in FIGS. **22** to **29** and in view of the about description with respect to FIGS. **18** to **21**.

[0142] In the exemplary fabricating method of the semiconductor device, if LDMOS devices are provided in an output port and an ESD protection device, the LDMOS devices may be fabricated using the same mask. The breakdown voltage of the LDMOS device in the ESD protection device may be made equal to or lower than the breakdown voltage of the LDMOS device in the output port. As such, the breakdown voltage of the LDMOS device in the ESD protection device may be kept equal to or lower than the breakdown voltage of the LDMOS device in the output port, e.g., all the time even